CLAIMS

What is claimed is:

1. A processing system including a processor, a main memory, and a cache configured to receive data from an address of the main memory upon a request for the data by the processor, the processing system comprising a crossbar interface between the processor and the cache.

2. The processing system of claim 1 wherein the main memory is controlled by a memory controller, the crossbar interface configured to link the memory controller, the processor and the cache.

3. The processing system of claim 1 wherein the crossbar interface comprises a plurality of ports via which the cache and the processor are linked based on the main memory address.

4. The processing system of claim 1 wherein the processor is configured to associate at least one main memory address range with the cache.

5. The processing system of claim 4 wherein the processor is linked with the cache based on an address range stored in the processor and corresponding to a range of addresses of the main memory mapped to the cache.

6. The processing system of claim 1 wherein at least one range of addresses of the main memory is mapped to the cache.

7. The processing system of claim 1 further comprising a plurality of caches, the processor comprising an address range table wherein each address range is associated with a cache.

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8. The processing system of claim 7 wherein the address range table is programmable to change at least one of an address range and a cache associated with the processor.

9. The processing system of claim 1 further comprising a plurality of caches, the processor comprising a plurality of address ranges and module identifiers corresponding to the caches.

10. The processing system of claim 9 wherein the crossbar interface comprises a plurality of ports, the crossbar interface configured to link a cache with the processor via a port associated with an address range in the main memory.

11. The processing system of claim 1 wherein the crossbar interface is configured to return the data requested by the processor to the cache and the processor in parallel.

12. The processing system of claim 1 wherein the crossbar interface comprises at least one crossbar.

13. The processing system of claim 1 further comprising a plurality of processors linked with the cache via the crossbar interface.

14. A processing system comprising a plurality of processors, a main memory, a plurality of caches, and a crossbar interface linking the caches and the processors, each cache configured to receive data from a range of the main memory upon a request for the data by one of the processors.

15. The processing system of claim 14 wherein the processors are configured to share at least one of the caches via the crossbar interface.

16. The processing system of claim 14 wherein the crossbar interface links one of the caches and one of the processors based on a module identifier supplied by the processor.

17. The processing system of claim 16 wherein the module identifier is associated by the supplying processor with a main memory address range.

18. The processing system of claim 14 wherein the crossbar interface is configured to provide signal synchronization for an asynchronous transaction between one of the caches and one of the processors.

19. The processing system of claim 14 further comprising at least one memory controller configured to send data from the main memory to a receiving cache and a requesting processor at the same time.

20. A method for configuring a multi-processor processing system comprising the steps of:

mapping a plurality of main memory address ranges to a plurality of caches;

mapping the caches to a plurality of processors; and

linking the processors and the caches using a crossbar interface.

21. The method of claim 20 further comprising the step of configuring a processor to interface with a cache to which is mapped a main memory address range addressable by the processor.

22. The method of claim 20 wherein the step of mapping the caches to a plurality of processors comprises associating, in a processor, a main memory address range with a module identifier for a cache.

23. The method of claim 20 wherein the step of mapping the caches to a plurality of processors comprises mapping a cache to more than one processor.

24. The method of claim 20 further comprising the step of changing a size of a cache, said step performed without changing the crossbar interface.

25. The method of claim 20 further comprising the step of configuring the processing system on a single die.

26. The method of claim 20 wherein the step of mapping the caches to a plurality of processors comprises mapping more than one cache to one processor.